Robust NVM Solutions for TSMC Specialty and Advanced FinFET Technologies

Sidense

ABSTRACT

The rapid progress in new Smart Connected ICs for IoT, mobile, automotive, industrial, and medical applications is driving the deployment of new specialty processes and smaller advanced technology nodes. Sidense's innovative, low-power non-volatile-memory (NVM) designs target these applications in TSMC's specialty (BCD, HV and CIS), ultra-low power (ULP) and FinFET processes.

With TSMC's leading-edge technologies, Sidense 1T-NVM supports the stringent requirements for a wide range of Smart Connected devices: operation from low-voltage sources with limited energy budgets, operation in harsh environments and robust, high-reliability operation over extended temperature ranges. Sidense has introduced solutions for TSMC specialty processes in BCD, CIS and ULP, optimizing the designs to cater to the various planar device varieties and features. Sidense has developed 1T-NVM for TSMC FinFET technologies with recently qualified offering for 16FF+ and support for the FFC variants. This introduces additional design elements for security options and for low-voltage operation while providing faster program performance and smaller footprints.

This presentation will cover how the latest 1T-NVM developments from Sidense address Smart Connected requirements with innovative designs for specialty processes and 3D bit-cell designs for advanced process nodes.

Version: 1.1

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Sidense™
Your Trusted Memory Partner

Sidense By The Numbers

- ~170 Engaged Customers
- ~670 Licenses
- ~170 Patents (Filed and pending)
- ~9 ~30 Fabs at multiple foundries
- ~19 ~60 Processes

Sidense's market-leading technology is validated by design wins with multiple Tier-1 customers and foundries, used in multiple advanced nodes and processes, and secured with IP patents granted in multiple jurisdictions

The Smart Connected Universe

- Devices and Systems that have some compute power and are networked, often wirelessly

IoT

Wearables

Mobile Computing

Medical

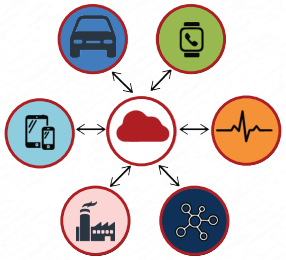
Industrial

Automotive

Edge Nodes
Sensing and Smart Devices (Data Gathering)

Hub Nodes
Sensor Fusion (Data Aggregation)

Central Computation
Cloud-Based Processing (Analytics and Action Drivers)

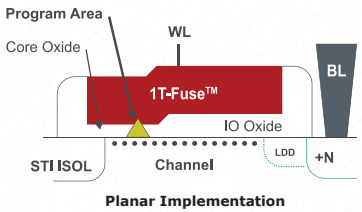


Smart Connected Demands

- Address a broad range of process nodes
- Operation from low-voltage sources with limited energy budgets
- Operation in harsh environments
- Robust, high-reliability operation over extended temperature ranges
- High level of security (for data, code and IP)

1T-Fuse™ | Split Channel Bit-Cell

- Reliably programmed through a controlled, non-reversible oxide breakdown
- Standard CMOS process
- Widespread industry adoption
- Proven silicon across all nodes from 180nm to 16nmFF for a range of TSMC's standard logic and specialty processes (BCD, HV, CIS, ULP, RF)



Planar Implementation

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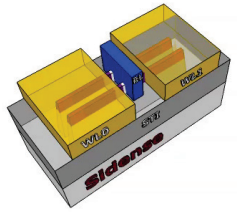
1T-NVM | TSMC FinFET technologies

- Same reliable bit-cell architecture suitable for FinFET 16nm and below
- Support for 16FF+ and 16FFC
- Features include
  - Security options
  - Low-voltage operation
  - Faster program performance
  - Smaller footprints



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1T-NVM | TSMC Specialty Process Support

- 1T-Fuse bit cell is easily portable to all TSMC specialty (BCD, HV, CIS) and FinFET technologies
  - The 1T-Fuse split-channel architecture is optimized for: low voltage, low leakage, high voltage, high tolerances, tighter/weaker DRM rules, etc.
- 1T-NVM makes maximum advantage of the process features
  - High voltage I/O cells in BCD
  - Low leakage in ULP
  - FinFET offers stronger PMOS devices that are used for programming, which reduces overall area and with less leakage

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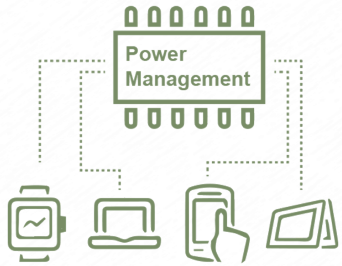
1T-NVM | TSMC Specialty Process Support

- Leader in High-Volume BCD/HV Applications
- Meets AEC-Q100 (Grades 1 & 0)
- ISO 9001 certified
- Available in 180BCD 5V only for cost-sensitive applications
- 180 BCD Gen 3 solutions in development
- Available for 130BCD 1.5V/5V designs



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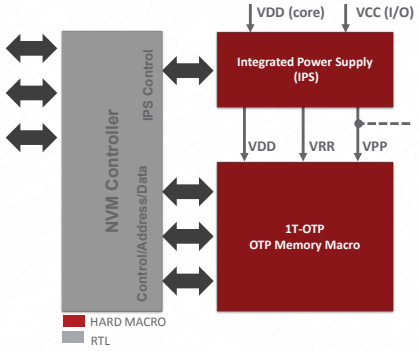
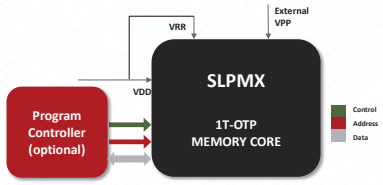
1T-NVM | A System Level solution

- OTP Memory Macro
  - Sidense 1T-Fuse bit-cells
  - Small footprint
  - Wide range of configurations from low to high densities
  - Physically Secure
- Power Supply Options
  - Integrated Power Supply (IPS)
  - Options for different power supply scenarios and use cases
  - Charge pump for programming
- Controller
  - Controls programming and test of OTP memory
  - Supports Test, ECID and eMTP
  - Additional security features



SLPMX | Designed for Low Voltage / Single Supply Read

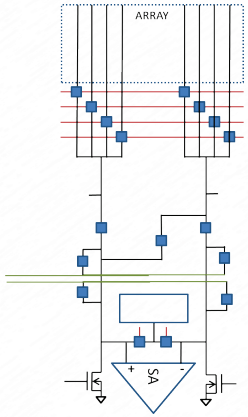
- 256 bits – 32 Kbits (logical bits)
- Single supply read
  - VRR=VDD=1.5V ±10%
- Fast Write
  - 100µs per word with (external VPP)
- Fast Read
  - 14ns read pulse in diff-redundant mode @VRR=1.5V
- Ultra-Low power consumption
  - 9µA/MHz



VDD=VRR=1.5V: NO IPS Required!

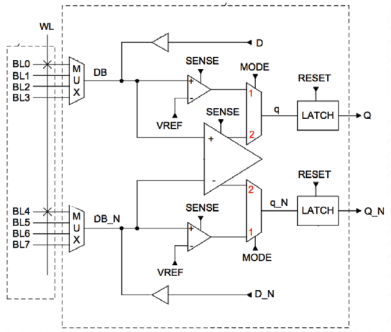
Low Voltage Operation

- Boost options
  - VGS, VDS
- Multi-read options
  - Redundant reads
  - Differential reads
  - Differential redundant reads
- Adjustable margin circuits
  - DACs
  - Reference generators



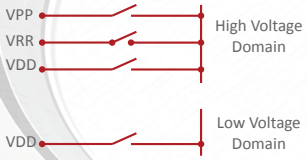
Flexibility | Security, Low Voltage Operation, Redundancy

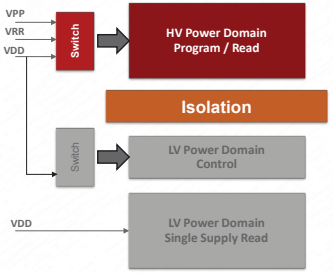
- Differential + Single-Ended SA options
- Secure Mode Options
  - Diff-Red + duplicate FULL data path
  - Diff mode + duplicate FULL data path
  - Diff mode + Power saving with single DP
- Q/NQ complementary output options
- Programmable SA offset
- Mixed read mode options
  - SE read or DIFF read
  - SE read + SE SA
  - SE read + DIFF SA



Harsh Environment | High Reliability Operation

- OTP Power Switch circuits
  - BCD & HV
- Voltage domains
  - High; VPP, VIO
  - Low; Core VDD
- Power On Reset Block (PORB)





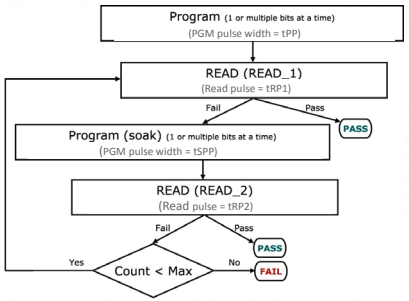
1T-NVM | High Reliability Testing

- ISO-9001 Certified
- Automotive Service Pack
  - Enabling ISO-26262
  - AEC-Q100 Grade 1 (125°C) and AEC-Q100 Grade 0 (150°C)
  - DFMEA
  - Extended support and warranty
- Over 10 years operation
- Long Term Data Retention (TDDB Testing)
- Trend to higher temperature operation >185°C and >10 years operation

Qualification Tests	
Early Life Failure Rate (ELFR)	AEC Q100-008
High Temperature Operating Life (HTOL)	JESD22-A108
High Temperature Storage Life (HTSL)	JESD22-A103
Time Dependent Dielectric Breakdown (TDDB)	Long Term Data Retention tests

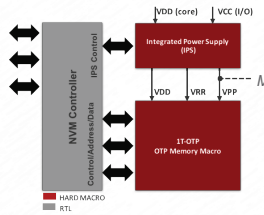
1T-NVM | Highly Efficient Program Algorithms

SLPMX Programming Algorithm

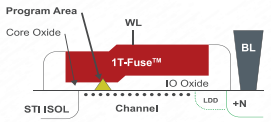


1T-Fuse™ | Designed for Secure Applications

- Sidense OTP Memory System
  - Designed for Secure boot code, HDCP and other secure key storage applications
- Security confirmed by multiple independent laboratories
- Physically Secure
- Architectural Security



Sidense OTP Memory System



Patented 1T-Fuse™ Split-Channel Bit Cell

1T-NVM bit cell | Inherently Physically Secure

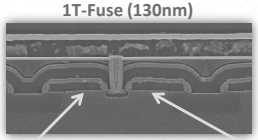
- Programming through permanent structural change in few atomic layers (far from diffusion)
- No isolated diffusion nodes exposed for attack
- No physical attack can reveal programmed state in FinFET or HKMG
- No leakage in non-programmed state
- State cannot be changed through exposure to high temperature, voltage or radiation
- No charge or voltage involved in state retention (unlike floating gate NVM, e.g. flash)
- State (even for a few bits) is virtually impossible to detect using physical attack or reverse engineering techniques

Typical eFuse

Non-Programmed Programmed

William Tonti "eFuse Design and Reliability"

1T-Fuse (130nm)



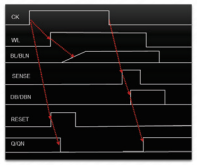
Non-Programmed Programmed

Tamper Resistance | Secure by Design

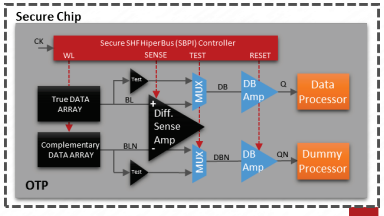
- Built-in redundant and/or differential mode
  - Highest read margins at wide operating voltage and temperature range
  - Prevents tampering using ambient conditions
- Built-in read timer
  - Prevents tampering with clock speed or access cycle
- Built-in hidden ROM / test OTP address space
- Built-in temperature compensation in IPS
  - Read voltage automatically adjusted to detected junction temperature – prevents any form of attack through high/low temperature exposure
- No shift registers
  - No stored data
- Delayering protection techniques
  - Routing to disable access with partial metal removal

Power Signature Proofing Techniques | Secure by Design

- Implemented in new 16FF designs
  - Can be applied to other architectures / nodes
- Fully differential data storage
  - Differential Read and Write
  - Differential Sense amplifier
  - Differential Data Output
  - Differential verify and test
- Exactly same Read timing waveform regardless of data content
  - No power signature regardless of access mode or programming state

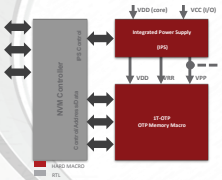


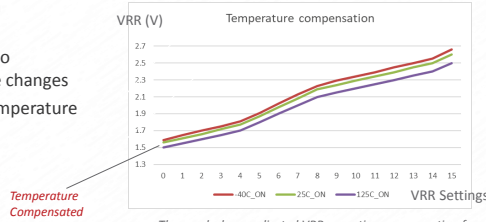
Fully Differential Read Sequence Waveforms



Temperature Compensation | Secure by Design

- Built-in temperature compensation in Integrated Power Supply (IPS)
- Read voltage automatically adjusted to compensate for junction temperature changes
- Prevents attacks through high/low temperature exposure

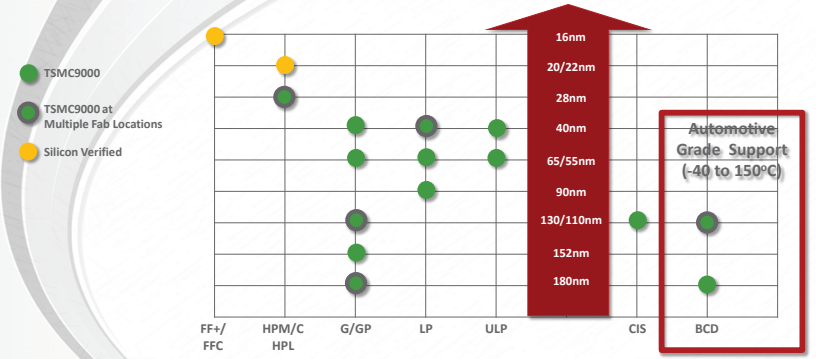




Temperature Compensated

The graph shows adjusted VRR operation compensating for temperature changes

Sidense 1T-NVM | TSMC Process Coverage



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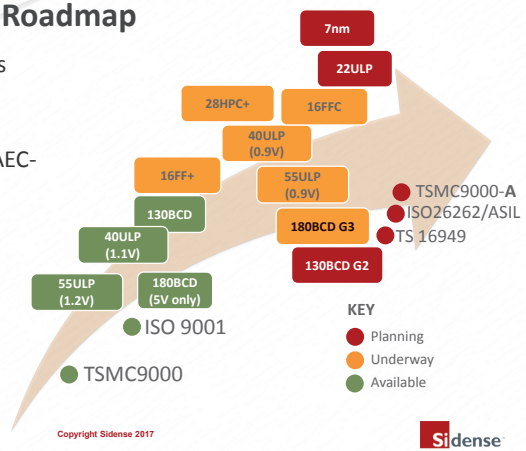
1T-NVM | 18-Month Roadmap

- Range of products for TSMC's automotive, Mobile and IoT platforms
- New qualifications to cover AEC-Q100 Grade 0/1 and ELFR
- TSMC9000-A
- Standards
  - ISO9000 Certified
  - TS 16949 under consideration
  - Enabling ISO26262/ASIL



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Summary

- Sidense 1T-NVM meets the demands of the Smart Connected Universe:
  - Provides low-voltage, low-power operation
  - High reliability even in harsh environments
  - Built-in secure storage and anti-tampering features
- Support for TSMC Specialty and FinFET Processes
- Roadmap supported by continued Investment in 1T-NVM for new TSMC processes

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